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FREQUENCY-DEPENDENT ELECTRICAL CHARACTERISTICS OF Al/Er_2O_3/SiO_2/n-Si/ Al MOS CAPACITOR DEPOSITED BY E-BEAM

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Abstract. *The aim of this paper is to investigate the frequency-dependent electrical characteristics of the Al/Er_2O_3/SiO_2 /n-Si/ Al MOS capacitor deposited by the e-beam PVD technique. The Er_2O_3/SiO_2 films were annealed in the nitrogen ambient for 30 min at 550 °C. The crystal structure and surface morphology of thin films have been investigated by XRD and AFM. The capacitance-voltage(C-V) and conductance-voltage (G/w-V) measurements have been performed in the frequency range of 50kHz-1MHz at room temperature. Furthermore, the frequency effects on the series resistance and interface state density through C-V and G/w-V curves were studied and analyzed. It has been observed that the series resistance gives a peak for each frequency, decreasing and disappearing with increasing frequencies. Also, it has been shown that the density of interface states increases with increasing frequency. The measured and calculated results reveal that the frequency has a significant impact on both R_s and D_{it} of the fabricated MOS characteristics. These effects are supposed to occur because of the interfacial layer (SiO_2) that is contained in between n-Si and Er_2O_3.*

Keywords: *Er_2O_3 thin films, series resistance, interface states density, and E-beam*

1. INTRODUCTION

Metal oxide semiconductor (MOS) structures are the essential part of many modern electronics. As the name suggests, they are made of a metal and a semiconductor separated by an interfacial layer. Their main task is to operate as an on/off switch, giving the device two conditions which can be used in logic operations [1–3]. As the device feature size continuously scales down to the nanometric regime, the traditional gate oxide (SiO_2) thickness approaches down to 2nm. A further scaling down in thickness raises issues such as excessive leakage current density, the high-power consumption of the devices, and errors in the logic devices. Substituting the existing SiO_2 material with high dielectric(k) material should exhibit similar electronic properties as SiO_2 but allows a higher physical thickness of the material. Recently, many high-k dielectric materials have been investigated and reported, such as Al_2O_3, HfO_2, Er_2O_3, Gd_2O_3, and ZrO_2 as a potential candidate to SiO_2. Among those investigated high-k dielectric materials, Er_2O_3 is an alternative to SiO_2 owing to its high-dielectric constant (k=10-14), a large bandgap (E_g=5eV), and a large conduction band offsets with Si (E_g=3.5 eV) [2, 4–6]. However, there are still some problems concerning the degradation of the metal–oxide-semiconductor device reliability which is because of the difficulty in finding a high-k material that has the perfect interface match with Si as compared to SiO_2. Besides, an interfacial layer (SiO_2) is grown on Si before the high-k layer to reduce lattice mismatch. Moreover, the interfacial layer could not only reduce the lattice mismatch but it would also increase the thermodynamic stability between high-k material and Si [4, 7]. To date, several techniques have been developed to grow Er_2O_3 thin films on a silicon substrate (Si) such as atomic layer deposition (ALD), chemical vapour deposition (CVD), E-beam evaporation and laser ablation. In the present work, the e-beam PVD technique has been employed because of its high and controllable rate of deposition, high density and homogeneity of the prepared thin films [4, 8]. Frequency-dependent MS, MIS and MOS structures have attracted large attention during the past decades and a variety of studies have been conducted by several researchers. However, frequency-dependent Al/Er_2O_3/SiO_2/n-Si/Al MOS deposited by the e-beam PVD technique has not yet been investigated [9–13].

The purpose of this work is to investigate the frequency-dependent electrical characteristics of the Al/Er_2O_3/SiO_2/n-Si/Al MOS capacitor deposited by the e-beam evaporation PVD technique and to determine electrical parameters such as diffusion potential (V_D), donor concentration N($_D$), Fermi energy level (E_F), and barrier height(Φ) by performing capacitance-voltage (C-V) and conductance-voltage measurements (G/ω-V). Also, the aim was to investigate the effects of series resistance and interface states through C-V and

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G/ω-V measurements in the frequency range of 50kHz-1MHz at room temperature.

2. Experimental details

To fabricate the MOS capacitors, a 6-inch 500μm-thick n-type Si (100) wafer with a resistivity of 2-4 Ωcm was cleaned using the Radio Corporation of America (RCA) method. Following the RCA method, the SiO_2 layer was grown on n-Si in a diffusion furnace by the dry oxidation method at 1000 °C. Then, the wafer was loaded into the electron beam evaporation chamber for Er_2O_3 thin film deposition. The base pressure of the chamber was below 4.8×10^{-4} Pascal and the substrate temperature was maintained at 250 °C. The Er_2O_3 thin films were deposited onto SiO_2/n-Si by evaporating a 4N pure Er_2O_3 target. The deposition rate was kept at about 1.5Å/s controlled by Inficon crystal sensors. The thickness of SiO_2 and Er_2O_3 layers was measured to be 20 nm and 130 nm with the help of the Angstrom Sun Spectroscopic reflectometer. The wafer was then divided into two portions, one was left as-deposited and the other one was annealed at 550 °C in N_2 atmosphere for 30 min. A shadow mask with the 1.5 mm diameter was used for the front contacts of the MOS capacitors formed by RF magnetron sputtering of aluminum (Al) for 60 min at the power rate of 120W. The back contact of the devices was formed with Al deposition for 40 min under the same conditions. The crystal structure and surface morphology were investigated by X-ray diffraction (XRD) and Atomic Force Microscopy (AFM). The capacitance-voltage (C-V) and conductance-voltage(G/ω-V) measurements were performed with the Keithley 4200-SCS Parameter Analyzer in the frequency range of 50kHz–1MHz at room temperature. Finally, all of the fabrication processes and the experiments were performed in Class-100 clean laboratories at the Bolu Abant Izzet Baysal University Nuclear Radiation Detectors Application and Research Center, Turkey.

3. Results and Discussion

3.1. Crystallinity

The crystal structure and phase identification of the films were confirmed by an x-ray diffractometer. Fig.1 shows XRD patterns of the Er_2O_3/SiO_2 thin films for the as-deposited and annealed at 550 °C. In the XRD spectrum of the as-deposited sample, one peak was found around 2θ=30° and one peak feature presented at 2θ=48.8°, which suggested that this sample is polycrystalline. However, annealed sample peaks were found at 2θ=30°, 33.9°, and 48.8°. These peaks were stronger than the ones found in the as-deposited which suggested that a better-crystallized Er_2O_3/SiO_2 was formed. It was observed that the preferred orientation of the fabricated films was in the cubic phase structure (222). The peaks were indexed by the International Center for Diffraction Data (ICCD card number 77-0777). The average grain sizes were investigated from the strongest of the (222) peaks using the well-known Scherer equation [14]:

$$D = \frac{0.9\lambda}{\beta\cos\theta} \qquad (1)$$

where λ (1.5418Å) is the wavelength of X-rays, D is the average grain size, β is the FWHM of the peaks corresponding to the (222) plane, and θ is Bragg angle at the peak position. The average grain size for as-deposited and samples annealed at 550 °C are found to be 11.0 nm and 10.7 nm, respectively. These results indicate that the degree of crystallization decreases with annealing temperature [15].

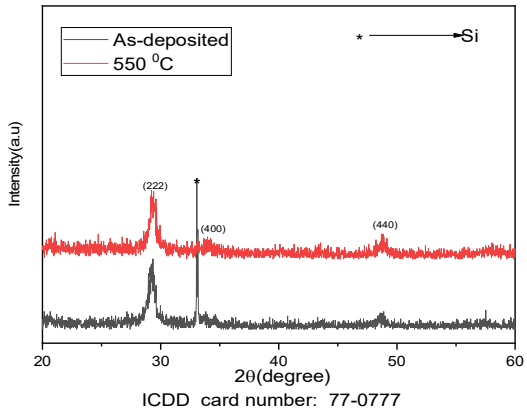

Figure 1. XRD spectra of Er_2O_3/SiO_2 thin films grown on Si (100) substrates (a) as-deposited and annealed in N_2 at 550 °C for 30 minutes.

3.2. AFM imaging

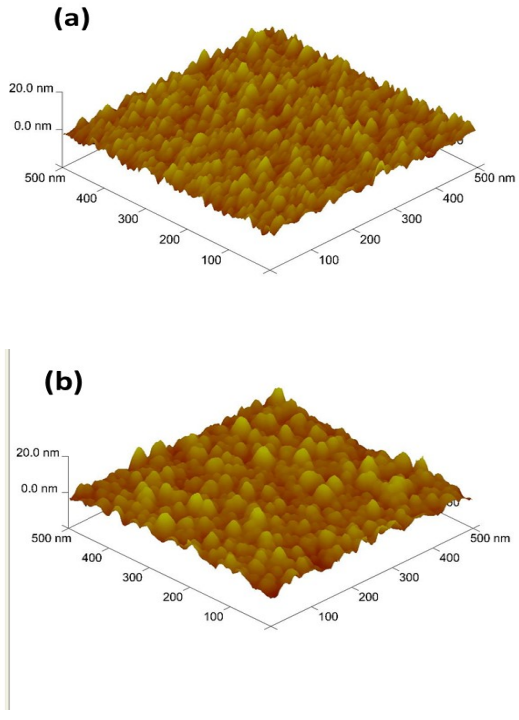

Figure 2. AMF image of Er_2O_3/SiO_2 thin films: (a) as-deposited and (b) annealed at 550°C

The surface morphology of the films was investigated by the atomic force microscopy (AFM). Fig. 2 shows the images of the as-deposited and the sample annealed at 550°C in three dimensions (3D) with the size of 5μm×5μm. The root mean square

(RMS) surface roughness values of the as-deposited and sample annealed at 550 °C are 1.82 nm to 1.98 nm. As seen in Fig. 2, the surface roughness value increase with annealing temperature. This is due to the increase in the grain size associated with high annealing temperature [4].

3.3. C-V and G/ω-V characteristics

The oxide capacitance can be calculated by the following equation:

$$C_{ox} = k\varepsilon_0 A / d \qquad (2)$$

where k is the constant of SiO_2 (3.9) or Er_2O_3(14) used for calculation, ε_O is the permittivity of free space (8.85×10^{-14} F/cm), A (1.77×10^{-2} cm²) is the area of the MOS capacitor and d is the thickness of the oxide (SiO_2(20nm) or Er_2O_3(130nm)). By using Eq. (2), the oxide capacitance of SiO_2 and Er_2O_3 were about 3.05×10^{-9} F and 1.69×10^{-9} F, respectively. As shown in Fig. 4 the total oxide capacitance of the Al/Er_2O_3/SiO_2/n-Si/Al MOS capacitor is equivalent to the series of the capacitance of the SiO_2 interfacial layer and the Er_2O_3 layer which can be described as

$$1/C_{ox} = 1/C_{SiO_2} + 1/C_{Er_2O_3} \qquad (3)$$

where C_{SiO_2} and $C_{Er_2O_3}$ are the oxide capacitance of the SiO_2 (3.05×10^{-9}F) and Er_2O_3(1.69×10^{-9}F). By substituting these values in Eq. 3, the total oxide capacitance of the MOS capacitor was found to be 1.09×10^{-9} F.

The capacitance-voltage (C-V) and conductance-voltage (G/ω-V) measurements were carried out to investigate the electrical characteristics of Al/Er_2O_3/SiO_2/n-Si/Al MOS capacitors. Fig. 3 shows the C-V curves of the Al/Er_2O_3/SiO_2/n-Si MOS capacitors in the frequency range from 50 kHz to 1MHz at room temperature. As shown in Fig. 3, the C-V curves at all frequencies show three regimes – accumulation, depletion, and inversion regions. The values of the capacitance in the accumulation region decrease with increasing frequency. At low frequencies, interface-trapped charges may be able to follow the ac signal and contribute to the measured capacitance in the accumulation region. However, for high frequencies, the interface-trapped charges hardly follow the ac signal. In other words, it means that these charges do not have enough time to respond to the fast ac signal. This is because their transport mechanisms are too slow compared to the ac signal [4, 5].

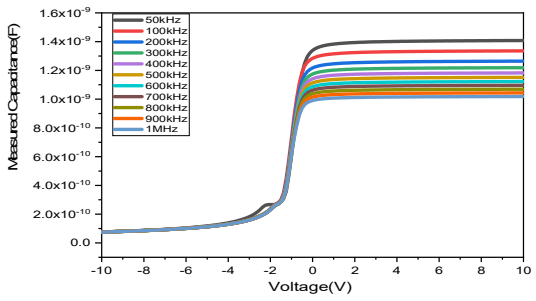

Figure 3. Capacitance-Voltage (C-V) curves of the Al Er_2O_3/SiO_2/n-Si/Al MOS capacitor for different frequency ranges from 50kHz to 1MHz

The conductance is an important parameter to investigate the interface quality of MOS structures; the conductance technique is based on the interactions between the interface trap charges and majority carrier densities in the semiconductor material (Si). As shown in Fig.4, the existence of series resistance (Rs) and SiO_2 cause the measured conductance-voltage (G_m/ω-V) increases with increasing frequency. This is attributed to the thickness and formation of the interfacial layer, series resistance and relaxation time of interface trap charges. The series resistance can affect Gm/ω–V measurements compared to the density of interface states because interface states can be eliminated at high frequencies [1, 13].

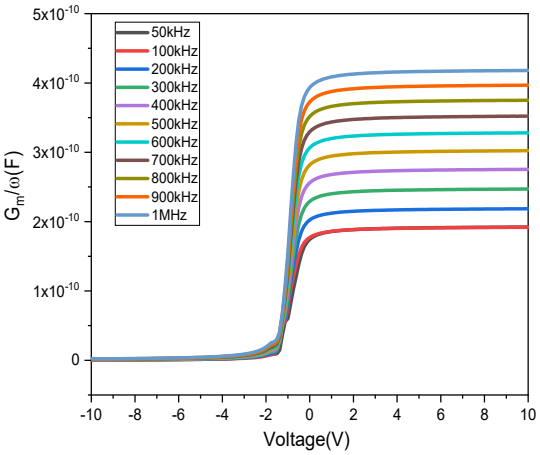

Figure 4. Conductance-Voltage (G/ω-V) curves of the Al/Er2O3/SiO2/ MOS capacitor for different frequency ranges from 50kHz to 1MHz

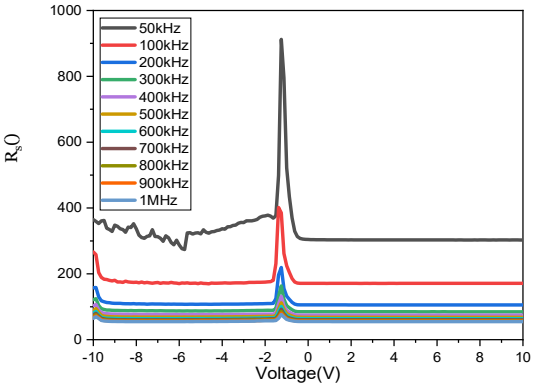

Figure 5. Series resistance curves of Al/Er_2O_3/SiO_2/Al MOS capacitor for different frequency ranges from 50 kHz to 1MHz

There are several techniques for obtaining the series resistance (Rs) of MOS structures in the literature. In this work, we used the conductance pioneered by Nicollian and Goetzberger. According to this technique, the real value of Rs can be obtained from Eq. (4)

$$R_s = \frac{G_m}{(G_m)^2 + (\omega C_m)^2} \qquad (4)$$

where ω=2πf is the angular frequency, (C_m) is the measured capacitance and (G_m) is the conductance

value in the strong accumulation region at high frequency (f≤500kHz). As seen in Fig. 5, the series resistance gives a peak for each frequency in the voltage range from -1.34V to -1.24 V, decreasing and disappearing with increasing frequency. This behavior shows that the interface trap may have enough energy to jump through traps between the metal (near contact) and the semiconductor in the Si bandgap. Besides, at high frequencies, the charges at the Er_2O_3/SiO_2 interface cannot be able to follow the ac signal because its transport mechanisms are too slow compared to the ac signal[16–18].

To remove the effects of series resistance (R_s) from the C-V and G/ω-V curves, the correction of the capacitance and conductance can be obtained by the following equations

$$C_c = \frac{[(G_m)^2 + (\omega C_m)^2]C_m}{a^2 + (\omega C_m)^2} \quad (5)$$

$$G_c = \frac{[(G_m)^2 + (\omega C_m)^2]a}{a^2 + (\omega C_m)^2} \quad (6)$$

where $a = (G_m) - [(G_m)^2 + (\omega C_m)^2]R_s$ (7)

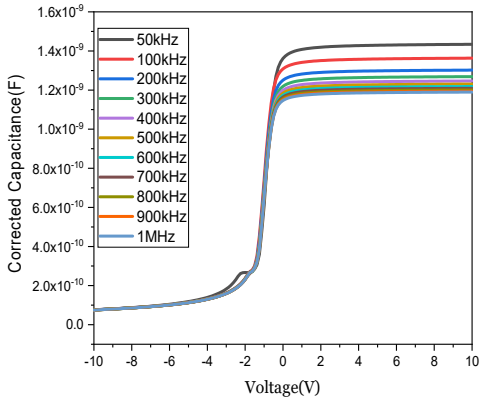

Figure 6. Corrected Capacitance-Voltage (C-V) curves of the $Al/Er_2O_3/SiO_2/Al$ MOS capacitor for different frequency ranges from 50 kHz to 1 MHz

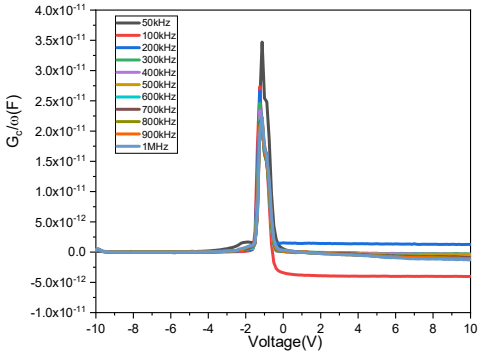

Figure 7. Corrected Conductance-Voltage (G_c/ω-V) curves of the $Al/Er_2O_3/SiO_2/n$-Si/Al MOS capacitor for different ranges from 50 kHz to 1 MHz

As shown in Figs. 6 and 7, the corrected C_c-V and G_c/ω-V curves of the MOS capacitor are measured in the voltage range from-10V to 10V. When the correction was performed on the C-V curves for the effect of series resistance, it was found that the values of the corrected capacitance (C_c) increase significantly as may be noted from Fig. 6. However, the corrected conductance (G_c/ω-V) curves have typical peaks for every frequency, while the peak magnitude decreases with increasing frequency, as shown in Fig. 7. This behavior may be dependent on the interface traps, relaxation time, the frequency of the ac signal [4, 6, 7].

Table 1. Some electrical parameters of the $Al/Er_2O_3/SiO_2/n$-Si/Al MOS capacitor.

Frequency (kHz)	V_D (eV)	E_F (eV)	$\Delta\Phi_B$ (meV)	Φ_B (eV)	N_D ($10^{15}cm^{-3}$)
50	1.470	0.250	18.50	1.230	1.87
100	0.948	0.249	16.90	0.716	1.99
200	0.927	0.249	16.80	0.695	1.99
300	0.917	0.249	16.80	0.685	1.98
400	0.909	0.249	16.70	0.677	1.98
500	0.899	0.249	16.70	0.667	1.97
600	0.895	0.249	16.60	0.663	1.97
700	0.886	0.249	16.60	0.653	1.97
800	0.883	0.249	16.60	0.651	1.97
900	0.880	0.249	16.60	0.648	1.97
1000	0.878	0.249	16.60	0.646	1.97

The density of interface states (D_{it}) at the $Er_2O_3/SiO_2/n$-Si interface is one of the most important parameters to investigate and it affects C-V and G/ω-V measurements. To determine D_{it}, several techniques have been suggested and the Hill-Coleman technique was among them. According to this technique, the density of interface states can be calculated by the following equation [12, 13].

$$D_{it} = (\frac{2}{qA})\frac{G_{c'}\max/\omega}{((G_{c'}/\omega)C_{ox})^2 + (1 - C_c/C_{ox})^2} \quad (8)$$

where q is elementary, A is the front contact area of the MOS capacitor, ω is the angular frequency, $G_{c,\max}/\omega$ are peak values of the corrected $G_{c,\max}/\omega$-V curve, and C_c is the corrected capacitance of the MOS capacitor corresponding to $G_{c,\max}/\omega$, and C_{ox} is the equivalent (total) capacitance of oxides. The D_{it} calculated from Eq. (8) as a function of frequency is shown in Fig. 7 and the obtained values are given in Table 2. As seen in Fig. 8, the density of interface states at $Er_2O_3/SiO_2/n$-Si interface increases with increasing frequency. This behavior is attributed to the slow type of interface trap charges. Also, the existence of the interfacial layer may cause interface states to increase with increasing frequency [14].

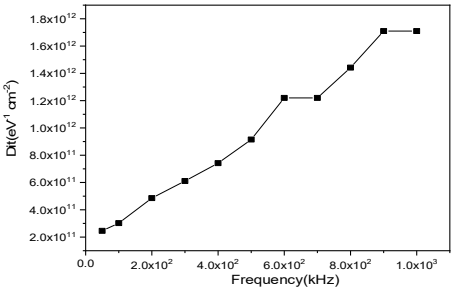

Figure 8. Variations of D_{it} as a function of frequency for the $Al/Er_2O_3/SiO_2/n$-Si/Al MOS capacitor

Table 2. Some electrical parameters of the $Al/Er_2O_3/SiO_2/n\text{-}Si/Al$ MOS capacitor.

Frequency (kHz)	C_C (10^{-9} F)	G/ω (10^{-11}F)	R_S (Ω)	D_{it} ($eV^{-1}cm^{-2}$)
50	1.43	3.42	900	2.46×10^{11}
100	1.36	2.65	398	3.02×10^{11}
200	1.30	2.59	217	4.85×10^{11}
300	1.27	2.40	161	6.11×10^{11}
400	1.25	2.32	130	7.42×10^{11}
500	1.23	2.19	111	9.15×10^{11}
600	1.21	2.17	100	1.22×10^{12}
700	1.21	2.16	91.0	1.22×10^{12}
800	1.20	2.16	85.0	1.44×10^{12}
900	1.19	2.14	77.0	1.71×10^{12}
1000	1.19	2.13	75.0	1.71×10^{12}

The depletion layer capacitance in MOS capacitors can be expressed as [9, 20]

$$C_c^{-2} = \frac{2(V_o + V)}{\varepsilon_s \varepsilon_o q A^2 N_D} \tag{9}$$

$$\frac{dC^{-2}}{dV} = \frac{2}{\varepsilon_s \varepsilon_o q A^2 N_D} \tag{10}$$

where ε_s (11.9 for Si) is the dielectric constant of the semiconductor, ε_o (= 8.85×10-14 F/cm) is the permittivity of the free space, q is the elementary charge, (A= 1.77×10^{-2} cm^2) is the area of the MOS capacitor, and N_D is the donor concentration of n-type Si, V is the applied voltage and Vo is the intercept of C_c^{-2} plot with the V axis and is given by [16]

$$V_o = V_D - \frac{kT}{q} \tag{11}$$

where V_D is the diffusion potential, k_B is the Boltzmann constant, and T is the absolute temperature. The value of the barrier height (Φ_B) can be obtained from the C_c^{-2}-V characteristics by the following famous equation [20]

$$\Phi_B = V_D + E_F - \Delta\Phi_B \tag{12}$$

where E_F energy is the difference between the bulk Fermi level and the conduction band edge and is given by [5, 6]

$$E_F = \frac{k_B T}{q} In(\frac{N_C}{N_D}) \tag{13}$$

where N_C (=2.82×10^{19} cm^{-3}) is the effective density of states for n-Si at room temperature and can be calculated by the following equation [17, 18]

$$N_C = 2\left[\frac{2\pi m^*_e m_o k_B T}{h^2}\right]^{3/2} \tag{14}$$

$$\Delta\Phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s\varepsilon_o}} \tag{15}$$

where E_m is the maximum electric field and can be obtained from the following well-known equation [4]

$$E_F = \sqrt{\frac{2qN_D V_O}{\varepsilon_s\varepsilon_o}} \tag{16}$$

Fig. 8 shows that the C_c-V plot is presented in the frequency range of 50 kHz to 1MHz. As it may be noted in Fig. 9, the line Cc-V plot is linear and changes for each frequency. This behavior is attributed to the donor concentration in the depletion, which indicates that the interface states cannot follow the ac signal especially at high frequencies. However, these traps can follow the ac signal at low frequencies and contribute to the measured capacitance. The electrical parameters, such as the diffusion potential (V_D) donor concentration (N_D), the Fermi energy level (E_F), and the barrier height (Φ), are obtained from the C_c-V plot for different frequencies and are given in Table 1. As shown in Table 1 in the frequency range of 50kHz to 1MHz, the C-V measurements revealed that the values of the barrier height change from 1.250eV to 0.838eV and the donor concentration from 1.85×10^{15} cm^{-3} to 1.95×10^{15} cm^{-3}. The Φ decreases with increasing frequency except at 50kHz – this is due to the reduction in the built-in potential (V_{bi}). Also, N_D decreases with increasing frequency except at 50 kHz. This behavior can explain whether the interface state charge contributes to the measured capacitance or the charge at the interface can follow applied voltage frequency [1, 6, 14, 16, 17].

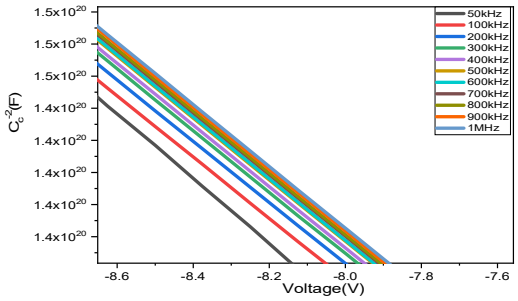

Figure 9. C_c^{-2}-V characteristics and the corresponding linear fit function of the $Al/Er_2O_3/SiO_2/n\text{-}Si/Al$ MOS capacitor at different frequency ranges from 50kHz to 1MHz

5. Conclusion

In this paper, we investigated the frequency dependent on the electrical characteristics of the $Al/Er_2O_3/SiO_2$ MOS capacitor deposited by the e-beam. The C-V and G/ω-V measurements were performed in the frequency range of 50kHz-1MHz. It is found that the capacitance in the accumulation region decreases with the increasing frequency, while the measured conductance increases with the increasing frequency. Furthermore, the frequency effects on the series resistance and the interface state density through C-V and G/w-V curves were studied and analyzed. It has been observed that the series resistance gives a peak for each frequency, decreasing and disappearing with increasing frequencies due to the distribution of interface states at $Er_2O_3/SiO_2/n\text{-}Si$. Also, it has been shown that the density of interface states increases with increasing frequency. The measured and calculated results reveal that the frequency has a significant impact on both R_s and D_{it} of the fabricated MOS characteristics. These effects are supposed to occur because of the interfacial layer

(SiO_2) which is contained in-between n-Si and Er_2O_3. Our results suggest that the Er_2O_3 gate dielectric is a promising alternative candidate to SiO_2.

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