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# FREQUENCY DEPENDENT ELECTRICAL CHARACTERISTICS OF Al/$SiO_2$/SiNWs/n-Si MOS CAPACITORS

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***Abstract***. *In this work, the frequency dependent electrical characteristics of Al/$SiO_2$/SiNWs/n-Si MOS capacitors were investigated. The electrical properties of the capacitors were calculated from the capacitance-voltage (C-V) and conductance-voltage ($G_m/\omega$-V) measurements for several frequencies ranging from 50kHz to 1MHz. Our experimental results showed that both frequency and voltage variations had a significant impact on the C-V and $G_m/\omega$-V characteristics. The C-V characteristics were found to decrease with an increase in the applied voltage frequency due to the distribution of the interface states ($N_{it}$) within the oxide layer. The $G_m/\omega$-V characteristics were also found to have peaks and the peaks increased with an increase in the applied voltage frequency except for 50kHz and 100kHz. This was caused by the existence of series resistance ($R_s$) and $N_{it}$. We have also studied the frequency dependence on the electrical parameters such as $R_s$, $N_{it}$, doping concentration ($N_D$), and barrier height ($\Phi_B$). The values of $R_s$ were found to decrease with increasing frequency, while the values of $N_{it}$, $N_D$ and ($\Phi_B$) were also found to increase with increasing applied frequency.*

***Keywords:*** *SiNWs, MOS capacitors, Series resistance, Interface states, C-V, $G_m/\omega$-V*

## 1. INTRODUCTION

Metal-Oxide-Semiconductor (MOS) capacitor is a key element of metal-oxide-field effect transistor transistors (MOSFETs), it consists of three layers namely; semiconductor layer, oxide layer which is generally of silicon oxide ($SiO_2$) and then metallic layer[1], [2]. Due to the oxide layer, MOS structure has been extensively investigated and applied not only electronics but also radiation sensors, solar cells productions[3–5]. However, MOSFETs and transistors as continue to shrink in size. This raises a large number of issues such as high leakage current density, high energy consumption and poor performance of the electronic devices[4],[5]. Therefore, one dimensional nanostructured materials such as silicon nanowires (SiNWs) are especially to overcome these issues due to their optical, electronic and magnetic properties. Moreover, SiNWs based capacitors possess high capacitance density value in the accumulation region compared to MOS capacitors without SiNWs. Therefore, this will help SiNWs based capacitors to store more energy and to reduce the power consumption significantly, and increase the speed in electronics devices[3], [4].

Several researchers have reported the fabrication of MOS capacitors using SiNWs [3],[5]. For instance, P.H. Morel *et al.* fabricated MOS capacitors using SiNWs and $Al_2O_3$. The high-k dielectric material was deposited by atomic layer deposition (ALD) technique. They were able to achieve the capacitance density of 18μF/cm² [6]. However, they indicated that using the ALD technique for the fabrication of SiNWs based devices requires chemical vapor deposition (CVD) technique, which have to operate at higher temperature process of about 400°C. It is very hard to control the diameter and doping of the nanowires. Moreover, this technique requires expensive equipment's and dangerous gases. This leads to the degradation of the devices based on nanowires [4],[7]. Therefore, in this study we employed the metal assisted chemical etching (MACE) technique for the fabrication of SiNWs, in order to apply them in MOS devices. This technique has attracted research interests in recent years, due to its low cost, simple and scalable with good repeatability. In addition, in this technique one can be able to control doping, shape, orientation and the high aspect ratio of the resulting nanowires [3],[4]. Other researchers reported that if they could control different parameters such as dielectric thickness, capacitance density, dielectric material, length never before could be achieved with good controllability. They also reported that MACE-SiNWs MOS capacitors have such potential with simplest fabrication process[4].

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For instance, E. Hourdakis *et al.* reported the fabrication of MACE-SiNWs MOS capacitor using 6nm $SiO_2$ as the dielectric material. They found that 2.5µm SiNWs capacitor had a highest capacitance density compared to the MOS capacitor without SiNWs [5]. Other researchers have also reported the fabrication of MACE -SiNWs based MOS capacitors using $Al_2O_3$, $TiO_2$ and $Al_2O_3/TiO_2/Al_2O_3$ (A/T/A) as the high-k dielectric materials. They found that MOS capacitor with $Al_2O_3/TiO_2/Al_2O_3$ had the highest capacitance density compared to other capacitors[4]. However, to the best of our knowledge, there is no work about frequency dependence on the electrical characteristics of SiNWs based MOS capacitors[8], [9]. Therefore, it is very much benefit to investigate the electrical properties of MOS capacitors based on SiNWs. Because SiNWs possess large surface area to volume ratio (S/A) which is resulting in the SiNWs based capacitors to store more energy and increase the capacitance density value in the accumulation region as reported by previous studies [4], [5]. Also, they will help to reduce the power consumption significantly and to increase the speed in the electronic devices.

The aim of this study is to investigate the frequency dependence on the electrical characteristics of the Al/$SiO_2$/SiNWs/n-Si MOS capacitors. The capacitance-voltage (C-V) and conductance-voltage ($G_m/\omega$-V) measurements were investigated in the frequency ranging from 50kHz-1MHz. The frequency dependence on the electrical properties of the SiNWs based capacitors were also investigated in details.

## 2. Experimental Details

SiNWs MOS capacitors were fabricated on n-type Si (100) wafers with the resistivity of 2-4 Ω cm. After standard RCA cleaning process, the backside of the samples was coated with the positive photoresist. The Si wafers were immersed into the solution of $AgNO_3/HF/H_2O$ (0.042g/9.6 ml/90.4ml) for 1min to deposit silver nanoparticles (AgNPs). The samples were then dipped in the solution of $HF/H_2O_2/H_2O$ (4ml/1ml/40ml) for 30min, to etch the Si wafers. Then, the samples were dipped in the mixed solution of $HNO_3/H_2O$ (20ml/20ml) for 10min to remove the AgNPs. Before the growth of $SiO_2$, the samples were immersed in 5% of HF and $H_2O$ for 3min. Followed by rinsing them with deionized water and dried with $N_2$. Afterwards, the samples were transferred to the diffusion furnace for the growth of $SiO_2$. The $SiO_2$ layer was grown onto SiNWs/ n-Si (100) by using dry oxidation method at 1000°C for 30min. The thickness of the $SiO_2$ was measured with the help of Sun spectrometer reflectometer and was found to be 110nm. Before the fabrication of SiNWs based capacitors, the oxide layer at the backside of the samples was removed by HF (5%) and $H_2O$.

The samples were then loaded in the RF sputtering technique for the formation of MOS devices. The front contacts ($1.77\times10^{-2}$ $cm^2$) were formed with shadow mask using RF magnetron sputtering of Al for 40min. On the other hand, the back contact was formed by Al deposition for 40 min with similar condition but without a shadow mask. Lastly, the MOS capacitors were annealed in $N_2$ ambient at 450°C for 40min in order to reduce the interface trap charges. The fabricated MOS capacitor is given in Fig 1. The C-V and $G_m/\omega$-V measurements were performed in the frequency of 50kHz-1MHz. The DC voltage was done in the range of -30V and +30V with a step voltage of 0.125V. The amplitude of the AC voltage was set at 30mV. The measurements were conducted using Keithley 4200-SCS Parameter analyzer instrument at room temperature, respectively.

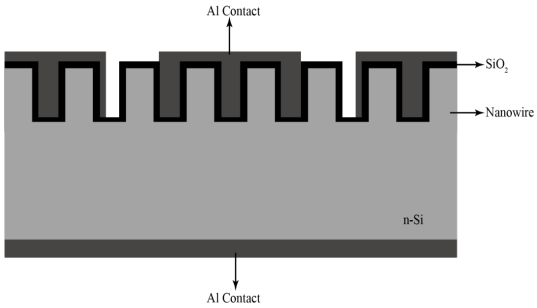


Figure 1. Schematic representation of the fabricated SiNWs based MOS capacitor.

## 3. Results and Discussion

### *3.1. Surface Morphology of SiNWs*

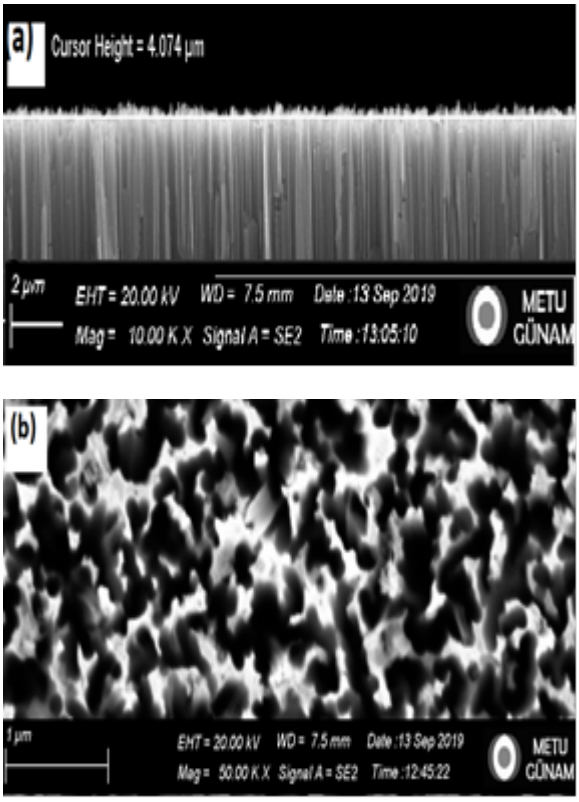


Figure 2. Cross section (a) and (b) top view SEM images of SiNWs etched in $HF/H_2O_2/H_2O$ for 30 min.

The surface morphology of SiNWs was studied by scanning electron microscope (SEM) technique. Fig.2(a), shows cross section and (b) top view SEM image of fabricated SiNWs. As shown in Fig.2(a), it can be clearly seen that the fabricated SiNWs are relatively straight and their length is about 4.074µm and similar results have been reported [7], [10],[11].

### *3.2. C-V and $G_m/\omega$-V characteristics*

The C-V and $G_m/\omega$-V measurements were carried out to study frequency dependence on the electrical characteristics of Al/$SiO_2$/SiNWs/n-Si/ MOS capacitor. Fig 3(a), shows the C-V curves of Al/$SiO_2$/SiNWs/n-Si MOS capacitor at various frequency ranging from 50kHz to 1MHz. It can be clearly seen that each of these C-V curves has three different sections which correspond to different regimes namely: accumulation, depletion, and inversion regime. The capacitance value in the accumulation region decreases with increasing in the applied voltage frequency as shown in Fig(3a).

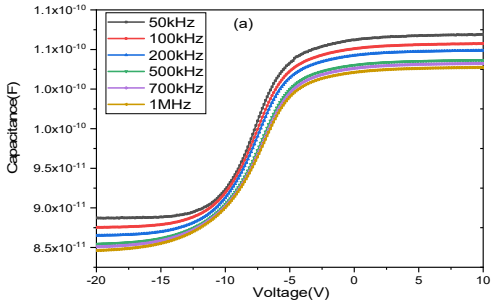


Figure 3(a). Capacitance-Voltage (C-V) curves of Al/$SiO_2$/SiNWs/n-Si MOS capacitor for different frequency.

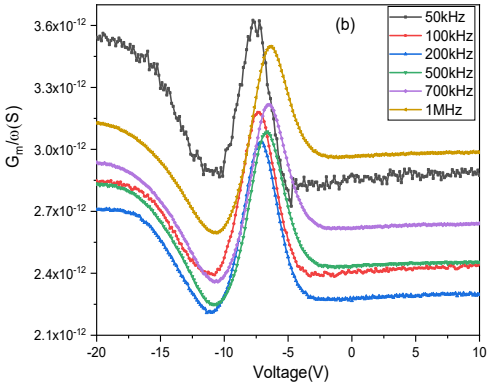


Figure 3(b). conductance-voltage (G/ω-V) curves of Al/$SiO_2$/SiNWs/n-Si MOS capacitor for different frequency.

This can be attributed to the interface states charges. When the C-V measurements have been taken especially at low frequency of 50kHz. During this frequency the interface states can easily follow the alternating signal which is resulting in the increase of the capacitance value [12], [13]. On the other hand, if the C-V measurements have been taken at high frequency of 1MHz, the surface states cannot follow the ac signal and hence they could not have any significant impact on the accumulation capacitance to due their higher life time than $1/2\pi f$ [12], [14].

The conductance method based on the conductance loses due to the interaction between the majority carrier band of the semiconductor and the surface states when a small ac signal is applied to the MOS device[13], [15]. Fig 3(b), shows the $G_m/\omega$-V curves of Al/$SiO_2$/SiNWs/n-Si MOS capacitor at various frequency ranging from 50kHz to 1MHz. It is clearly seen that $G_m/\omega$-V curves possess strong peaks and the peaks are located between -10.5V and -3.25V. On the other hand, the $G_m/\omega$-V peaks increase with an increase in the applied voltage frequency except for 50kHz and 100kHz. This behavior of the peaks could be attributed to the existence of series resistance ($R_s$) and the distribution of surface states within the oxide layer [14], [16]. Moreover, and as stated above, the surface states can easily follow ac signal especially for low frequency measurements compared to high frequency measurements due to their higher lifetime than $1/2\pi f$ [13], [16]. Therefore, this may contribute to the measured $G_m/\omega$-V curves of the fabricated MOS capacitor.

Several methods have been developed for calculating the value of series resistance ($R_s$). In this paper we used the method developed by Nicholllian [1]. The values of the $R_s$ were calculated by the following equation.

$$R_s = \frac{G_m}{(G_m)^2 + (\omega C_m)^2} \qquad (1)$$

where $C_m$ and $G_m$ are measured capacitance and conductance values extracted from the strong accumulation and $\omega=2\pi f$ is the angular frequency. Fig 4(a), shows series resistance-voltage ($R_s$-V) curves of Al/$SiO_2$/SiNWs/n-Si MOS capacitor at various frequency ranging from 50kHz to 1MHz. It is observed that $R_s$ gives a peak between -9.38V and -3.34V depending on the applied voltage frequency. The $R_s$ peak also decreases with an increase in the applied voltage frequency. We can consider that the surface states have sufficient energy to move from the traps located between the metal and the semiconductor interface in the energy band gap of the silicon[17], [18].

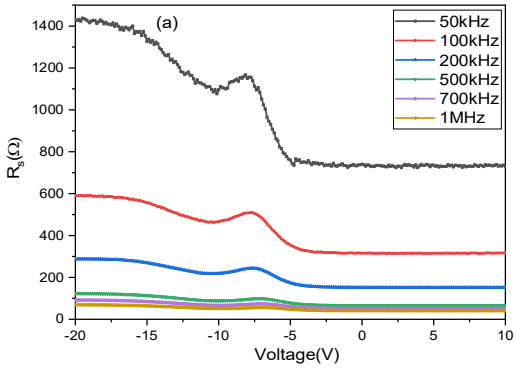


Figure 4. (a) series resistance-voltage (Rs-V) curves of Al/$SiO_2$/SiNWs/n-Si MOS capacitor for different frequency

Conductance method is one of the easiest methods to determine the value of interface states ($D_{it}$). This method was developed by Hill-Coleman[1], [19]. The value of $D_{it}$ can be calculated from the following expression.

$$D_{it} = \left(\frac{2}{qA}\right)\frac{G_{c'}\max/\omega}{((G_{c'}/\omega)C_{ox})^2 + (1 - C_c/C_{ox})^2} \qquad (2)$$

where $q$ is the electronic charge, $A$ is the area of the MOS device, $G_c/\omega$ is corrected conductance corresponding to the maximum peak, $C_c$ is the corrected capacitance and $C_{ox} = C_{acc}$ is the oxide capacitance in the accumulation regime. Fig.(4b), shows the interface states density depending on the frequency for the Al/$SiO_2$/SiNWs/n-Si MOS capacitor. We can see the value of $D_{it}$ to increase with an increase in the applied frequency. The increase in the value of $D_{it}$ is caused by slow type of trap charges and the etching effect may also contribute to the value of surface states density [13], [20]. Other researchers have reported the fabrication of MACE-SiNWs MOS device using 6nm $SiO_2$ as the dielectric material and the value of $D_{it}$ was found to be $5.0\times10^{10}$ $eV^{-1}$ $cm^{-2}$ [5]. However, this value is less than the $D_{it}$ value ($6.75\times10^{12}eV^{-1}$ $cm^{-2}$) obtained in this work. This could be due to different experimental conditions such as annealing ambient, temperature, deposition time, etc. Therefore, these factors may contribute to this behavior of $D_{it}$ value.

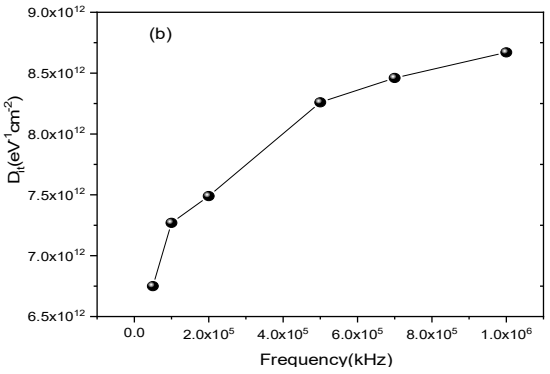


Figure 4. (b) Interface states density as the function of frequency for Al/$SiO_2$/SiNWs/n-Si MOS capacitor.

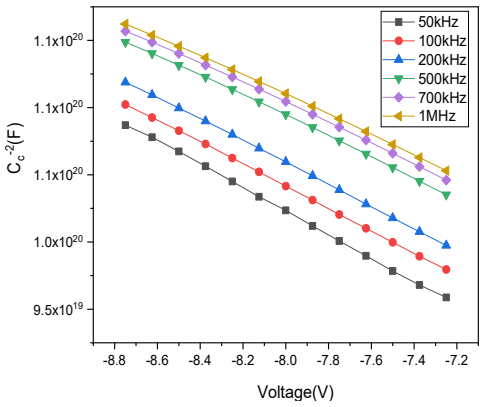


Figure 5. Corrected Capacitance Squared-Voltage ($C_c^{-2}$-V) plot of Al/$SiO_2$/SiNWs/n-Si MOS capacitor for various frequency.

The capacitance of the MOS capacitor in the depletion layer is given by[12], [17].

$$C_c^{-2} = \frac{2(V_o + V)}{\varepsilon_s \varepsilon_o q A^2 N_D} \qquad (3)$$

where $V$ is the applied voltage, $\varepsilon_s$ is the dielectric constant of Si and which is about 11.9, is vacuum permittivity ($8.85\times10^{-14}$ $F/cm^{-2}$), $N_D$ is the donor concentration, $V_o$ is the built potential, while other parameters have already been defined in Eq. (2). The value of $V_o$ can be obtained from [17], [18].

$$V_o = V_D - \frac{kT}{q} \qquad (4)$$

The value of the barrier height was calculated using the following equation[14], [16], [21].

$$\Phi_B = V_D + E_F - \Delta\Phi_B \qquad (5)$$

The values of Fermi energy and image force barrier lowering were obtained from [13], [18], [21].

Table 1. Summary of the electrical parameters obtained at various frequency of 50kHz to 1MHz for Al/$SiO_2$/SiNWs/n-Si MOS capacitor.

| Frequency (kHz) | $V_D$ (eV) | $E_F$ (eV) | $\Delta\Phi_B$ (meV) | $\Phi_B$ (eV) | $N_D$ ($10^{15}cm^{-3}$) |
|---|---|---|---|---|---|
| 50 | 3.75 | 0.23 | 28.73 | 3.95 | 4.34 |
| 100 | 4.64 | 0.23 | 30.76 | 4.84 | 4.59 |
| 200 | 5.03 | 0.23 | 31.47 | 5.22 | 4.65 |
| 500 | 6.43 | 0.23 | 34.05 | 6.62 | 4.98 |
| 700 | 6.91 | 0.22 | 34.90 | 7.10 | 5.11 |
| 1000 | 7.24 | 0.22 | 35.48 | 7.43 | 5.20 |

Fig. 5, shows the corrected capacitance squared-voltage ($C_c^{-2}$-V) plots of Al/$SiO_2$/SiNWs/n-Si MOS capacitor at various frequency ranging from 50kHz to 1 MHz. It is clearly seen that; the $C_c^{-2}$-V plots is linear at a given frequency as shown in Fig 5. This linearity is due to the distribution of interface trap charges [13], [17].The value of $\Phi_B$ and $N_D$ was obtained from the $C_c^{-2}$-V plot. As can be seen in Table 1, the value of $\Phi_B$ is between 3.95eV and 7.43eV, while the value of $N_D$ is between $4.34\times10^{15}$ $cm^{-3}$ and $5.20\times10^{15}cm^{-3}$. The increase in the value of $\Phi_B$ with increasing frequency is attributed to an increase in the value of diffusion potential($V_D$)as suggested earlier [13].

## 4. Conclusion

In this paper, we have studied frequency dependence on the electrical characteristics of Al/$SiO_2$/SiNWs/n-Si MOS device through C-V and $G_m/\omega$-V measurements at various frequency ranging from 50kHz to 1MHz. It was found that the value of capacitance decreased with an increase in the applied frequency, while the $G_m/\omega$-V had peaks and these peaks decreased with an increase in the applied voltage frequency but except for 50kHz and 100kHz. This could be attributed to the existence of $R_S$ and

distribution of $D_{it}$ within the oxide layer. We also studied the frequency dependence on the electrical parameters of the device. It was observed that the frequency had a huge influence on both $R_s$ and $D_{it}$. On the other hand, we also found that the value of $D_{it}$, $N_D$ and $\Phi_B$ increased with an increase in the applied frequency. Moreover, our results show that MACE-SiNWs based devices are promising materials especially in various fields but more research is needed.

The future work will be based on the fabrication of SiNWs based MOS capacitors using high-k dielectric materials. The MOS capacitors will be exposed to low and high doses, respectively. Therefore, this will help us to understand the effect of gamma radiation on SiNWs based capacitors with high-k dielectric materials.

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